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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/972,041	10/05/2001	Steven Teig	SPLX.P0068	5250
23349	7590	02/12/2004	EXAMINER	
STATTLER JOHANSEN & ADELI			ROSSOSHEK, YELENA	
P O BOX 51860			ART UNIT	
PALO ALTO, CA 94303			PAPER NUMBER	

2825

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/972,011

**Applicant(s)**

TEIG ET AL.

**Examiner**

Helen B Rossoshek

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 07 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 59-74 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 59-74 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### **DETAILED ACTION**

1. This office action is in response to the application 09/972,011 filed 10/05/2001 and amendment filed 11/07/2003.

2. Claims 58-74 remain pending in the application.

#### ***Claim Rejections - 35 USC § 112***

3. Claims 59-64 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification fails to show or describe to enable the limitation "determining a ratio of first interconnect ... to create a simulated Euclidean interconnect ... wiring angle". The rejection of these claims is based on the examiner's interpretation.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 59-74 are rejected under 35 U.S.C. 102(b) as being anticipated by Linsker (US Patent 4,782,193).

As to claims 59, 62, 65, 69 and 72 Linsker et al. teaches determining a preferred wiring angle for a metal layer of the integrated circuit layout by using principal wiring

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along a first direction to a second interconnect line length along a second direction that is approximately 45 degrees from the first direction to create a simulated Euclidean interconnect line along the preferred wiring angle in the light of calculating the ratio between connection length along the principal wiring direction (L45) and straight line length (EUCL) (col. 9, ll.59-65; col. 10, 1-3); routing the metal layer using the preferred wiring angle by creating interconnect wires made up of wire segments of the first interconnect line length along the first direction and wire segments of the second interconnect line length along the second direction as shown on the Fig. 3 and 4 wherein the principal wiring direction (first direction) ( $D_1 - D_{10}$ ) including the segments of the second direction which are 45 degrees related to the first direction considering that besides the various of the principal wiring directions there are wiring directions which are not parallel to the principal wiring direction ("wrong way") (col. 12, ll.15-26); determining a ratio of a first interconnect line length along a first direction to a second interconnect line length along a second direction that is substantially orthogonal to the first direction to create a simulated Euclidean interconnect line along the preferred wiring angle within the calculation of the ratio as MANH/EUCL, wherein the EUCL is a straight line, which is orthogonal to the preferred wiring direction as shown on the Fig. 7 where the segment SX (simulated Euclidean interconnect line) is perpendicular to the theoretical line  $OV_2$  and the segment SY is perpendicular to the theoretical line  $OH_2$  and might be at any angle to the preferred wiring direction (col. 11, ll.30-36) within the conception of the "wrong way" which is not parallel to the principal wiring direction in the plane and various of the combinations of the wiring arrangement of the wiring directions

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in the various of the sets of different wiring planes (col. 4, II.5-9; II.15-21; col. 12, II.15-26); a plurality of circuit modules (col. 1, II.6-7; col. 2, II.45-50); a first interconnect line, the first interconnect line layer having a preferred horizontal direction of interconnect lines as shown on the Fig. 1 the wiring plane (10) having the horizontal principal wiring direction (col. 5, II.50-54); a second interconnect line layer, the second interconnect line layer having a preferred vertical direction of interconnect lines as shown on the Fig. 2 wherein the wiring plane (20) has a vertical principal wiring direction (col. 5, II.64-66); and a third interconnect line layer, the third interconnect line layer having a first arbitrary diagonal preferred direction as shown on the Fig. 3 wherein the plane (30) has a diagonal principal wiring direction (45 degrees) (col. 6, II.7-9; II.14-26); wherein interconnect lines on the third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is approximately 45 degrees diagonal to the horizontal as shown on the Fig. 3 wherein the plane (30) has the interconnect lines ( $D_1$  -  $D_5$ ) with the subsegments with 45 degrees to the principal wiring direction; wherein interconnect lines on the third interconnect line layer comprise a plurality of alternating interconnect line subsegments wherein a first subsegment is horizontal and a second subsegment is substantially orthogonal to the horizontal using the conception of the "wrong way" which is not parallel to the principal wiring direction in the plane and various of the combinations of the wiring arrangement of the wiring directions in the various of the sets of different wiring planes (col. 4, II.5-9; II.15-21; col. 12, II.15-26).

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Moreover with respect to the claims 60, 61, 63, 64, 66, 67, 68, 70, 71, 73 and 74 Linsker et al. teaches the first direction is horizontal and the second direction is substantially 45 degrees from the horizontal; the first direction is horizontal and the second direction is vertical; within the conception of the "wrong way" which is not parallel to the principal wiring direction in the plane and various of the combinations of the wiring arrangement of the wiring directions in the various of the sets of different wiring planes (col. 4, ll.5-9; ll.15-21; col. 12, ll.15-26); a fourth interconnect line layer, the fourth interconnect line layer having a second diagonal preferred direction, the second diagonal preferred direction substantially orthogonal to the first diagonal preferred direction wherein interconnect lines on the fourth interconnect line layer comprises a plurality of alternating interconnect line subsegments as shown on the Fig. 4 wherein the wiring plane (40) has the second principal wiring direction ( $135^{\circ}$ ) (col. 6, ll.16-19); a fifth interconnect line layer, the fifth interconnect line layer having a second diagonal preferred direction, the second diagonal preferred direction substantially orthogonal to the first diagonal preferred direction wherein interconnect lines on the fifth interconnect line layer comprise a plurality of alternating interconnect line subsegments as shown on the Fig. 4 wherein the wiring plane (40) has the second principal wiring direction ( $135^{\circ}$ ) (col. 6, ll.16-19) and within the conception of the "wrong way" which is not parallel to the principal wiring direction in the plane and various of the combinations of the wiring arrangement of the wiring directions in the various of the sets of different wiring planes (col. 4, ll.5-9; ll.15-21; col. 12, ll.15-26).

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**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen B Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HR

  
A.M. THOMPSON  
MASTER'S LEVEL PATENT EXAMINER  
TECHNOLOGY CENTER 2800